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Film Qualification and Electrical Characteristics of Al Doped $PbTiO_3$ Ferroelectric Field Effect Transistors

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Abstract:— Polycrystalline $Pb(Ti_{0.94}Al_{0.06})O_3$, PTA6, a ferroelectric oxide was prepared by high temperature solid state reaction route. Fabrication process of a single-transistor type ferroelectric field effect transistor (1TFeFET) memory with (PTA6) film was prepared by non-expansive and unsophisticated techniques. The film qualification was studied from C^{-2} vs V linear graph. Ferroelectricity and non-volatility of PTA6 films were analysed by means of P-E hysteresis loop. Hysteresis loops measurement were performed with Sawyer-Tower circuit at 100 kHz and 10 V. Electrical characteristics (drain & transfer) of all films were measured. The FeFET with PTA6 at 600˚C exhibited the smallest value of threshold voltage (3.33V). The m^{th} power of PTA6 cell at 500˚C indicated the most suitable for parabolic behaviour. According to the experimental results, the laboratory prepared transistors were utilized for 1T of non-volatile ferroelectric random access memory (NVFRAM).

Keywords_ **Ferroelectric, Hysteresis, NVFRAM, PTA6, 1TFeFET**

1 Introduction

THE nonvolatile memory is a memory which retains store data even its external power supply is disconnected [1]. Nonvolatile is divided into ROM (Read-only-memory) that can be read and RAM (random-access memory) that can be read and written [2]. FRAM is a type of ferroelectric random access memory that uses a ferroelectric thin film. That is a promissing candidate for nonvolatile memory [3]. For the past two years, FRAMs have attracted much attention due to their potential advantages such as nonvolatility, unlimited write cycles and low power consumption [4]. Ferroelectric materials are being considered for application in different kinds of devices, such as storage information and photonic devices, piezoelectric actuators and infrared sensors [5]. The spontaneous polarization of ferroelectric materials implies a hysteresis effect which can be used as a memory function, and ferroelectric capacitors are indeed used to make ferroelectric RAM for computers [6]. Modified lead titanate compositions, perovskite–phase metal oxide, have recently been tested in the form of thin films aiming at electronic applications because of their piezoelectric, electro optic and pyroelectric properties [7-9].

Today, ferroelectric memories are moving from the laboratory to the market place. FRAM with one transistor and one capa citor (1T1C) per cell has been used for commercial application [10]. Nondestructive read out (NDRO) FRAM which has a transistor as a memory cell has high attention since the ferroelectric gate offers simpler circuits and excellent performance[11].

In this study, the author will report the fabrication process of a single-transistor type ferroelectric field effect transistor (1TFeFET), film qualification , ferroelectric memory behavior and output characteristics of Al (6mol%) doped $PbTiO_3$ thin film transistors.

2 EXPERIMENTAL PROCEDURE

The properties of the solid solution were strongly influenced by their preparation procedure. To prepare the sol-gel precursor solution, PbO, TiO_2 and Al_2O_3were used as starting materials. The purity of materials was 99.9% as analar grade. Each of these three materials was ground in agate mortar for three hours to form homogeneous grain size. To reduce the grain size, the powder was sieved with 3-stages mesh sieve (100 mesh, 250 mesh and 400 mesh). Then this sample powder was dispersed by the air-jet milling under the pressure of 40 lb/in^2 to obtain the moisture less particle and blander for 15 minutes with constant pressure to ensure good dispersion. And then the powder was grinded by ball-milling in 20 hours. Then they were mixed to get the chemical formula $PbTi_{(1-x)}Al_xO_3$ (x=0.06 mol%) powder. And then it was heated on 800˚C and 900˚C for 1 hour. The PTA powder (900˚C) was chosen for further investigation because of its smaller crystallite size (38.8 nm). Al doped $PbTiO_3$ were weighted and dissolved in 2 methoxyethanol solvent. The mixture solution was acidified with 3 mg of HCl. The solution was stirred and refluxed up to obtain precursor solution.

The substrate used for this study was p-Si (100), which were

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(0.5cm×1cm) and thickness of 280-300 μm. Before film fabrication, they were washed ultrasonically in distilled water. Then they were washed in boiling acetone and in boiled propenol for 5 minutes to remove greasy films. And then they were immersed in nitric acid for 5 minutes in order to remove ionic contamination. After that they were etched in buffered hydrofluoric acid for 5 minutes to remove oxide films. Finally the Si wafers were cleaned in distilled water and dried on flat oven at 100˚C in open air for a few minutes then the cleaned Si wafers were obtained.

SiO_2, as an insulating layer, was thermally deposited on p-Si (100) by heating at 1200˚C into the furnace about 1 hour. The middle zone of SiO_2/Si structure was covered with apiezon wax and the remaining zones were etched with HF: DI water (1:3) to remove SiO_2 layer totally. To fabricate source (S) and drain (D) regions, n type phosphorus was deposited on these layers and annealed at 550˚C for 1 hour.

By diffusion mechanism, S and D regions were obtained at the ends. And then, the precursor solution was deposited on middle zone of SiO_2 layer using spin coating to get gate region. So we obtained metal ferroelectric insulating semiconductor (MFIS) field effect transistor with PTA6 film. The three process temperatures (500˚C, 600˚C and 700˚C) were also performed according to examine the PTA film quality at different process temperatures.

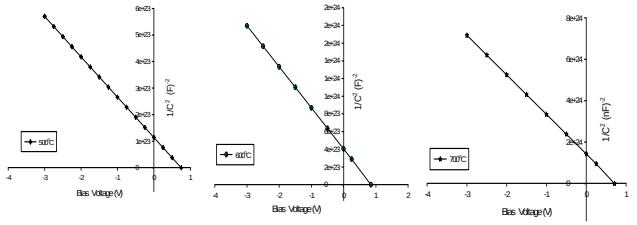
3 RESULTS AND DISCUSSION

3.1 C^{-2} vs V Characteristics

To examine the dopant concentration into mid-zone of FeFET with Si-body, C^{-2}-V characteristic of PTA films are essentially observed at different process temperatures and shown in figure 1 (a ~ c). From of C^{-2} –V characteristics plots, it is observed that enhancement is occurred in C^{-2} value with decrease in applied voltage drop across PTA6 film sandwiched between two Cu electrodes. This fact revealed that uniformity of $PbTiO_3$ and Al_2O_3 concentrations in fabricated films. The plot of C^{-2} –V gives a straight line from which possible to obtain V_{bi} whose intercept on the voltage axis and the slope can be used to measure the effective dopant concentration. The calculated value of built in potential (V_{bi}) barrier height ($Ø_{bo}$), the dopant concentration in p-type semiconductor (N_a), the dopant concentration in n-type semiconductor (N_d), the effective dopant concentration (N_i) and the depletion layer width (W) can be described in Table 1.

3.2 Thermal Hysteresis Characteristics (Non- volatile Memory)

In this study, the forward bias characteristic of the device ferroelectricity and non-volatility of fabricated PTA6 films were interpreted by means of P-E hysteresis loop. Hysteresis loop measurements were performed with Sawyer - Tower circuit at applied frequency 100 kHz and device voltage of 10V. PTA6 sample was served as circuit element and the loop was recorded on oscilloscope (YOKOGAWA ALSIO 50 MHz). Figure 2 (a~c) described the thermal hysteresis loop of MFIS cell with PTA6 film. All hysteresis loops were acceptable and has three complete points such as saturation, remanence and coercivity. If we first applied a small electric field, we will have only a linear relationship between electric field strength increased. Then a field strength decreased, the polarization would be generally decreased, but did not return back to zero. When the field was reduced to zero, the crystal would exhibit a remanent polarization (P_r). The extrapolation of the linear segment of the curve back to the polarization axis represented the value of the spontaneous polarization (P_s). The strength of the field required to reduce the polarization P to zero was called the coercive field strength (E_c). All hysteresis loops looked non-linear and silm. All measurable hysteresis parameters were quoted in Table 2. From the view point of digital electronics, PTA6 films could be used as a prototype of non-volatile memory application.

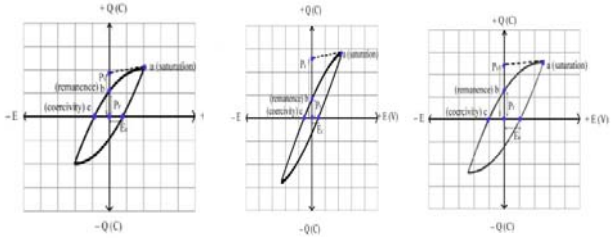


(a) (b) (c)

Fig .1 C^{-2} vs V characteristic of PTA6 FeFET (a) at 500˚C (b) 600°C and (c) at 700°C

Table .1 Some parameters derive from the analysis of C^{-2}- V characteristics

Temperature (˚C)	500	600	700
slope	1.52E+23	9.74E+23	1.91E+24
$Ø_{bo}$ (eV)	1.06	1.19	1.09
V_{bi} (V)	7.50E-1	8.50E-1	7.10E-1
N_a (cm^{-3})	7.83E+15	2.56E+15	6.20E+15
N_d (cm^{-3})	1.13E+17	1.66E+19	3.04E+17
N_i (cm^{-3})	7.33E+15	2.56E+15	6.19E+15
C_{max} (F)	1.32E-12	7.46E-13	3.73E-13
W (cm)	7.92E-5	1.40E-4	2.80E-4



(a) (b) (c)

Fig. 2 Thermal hysteresis loop of MFIS cell with PTA6 film (a) at 500˚C (b) 600ºC and (c) at 700ºC

Table .2 Hysteresis parameters for PTA6 films at different temperatures

Process temperature(°C)	P_s(μC/cm²)	P_r(μC/cm²)	E_c (kV/cm)
500	**14.3**	**3.25**	**6.9**
600	**13.5**	**3.38**	**6.6**
700	**14.1**	**3.38**	**6.6**

3.3. Electrical Characteristics Measurement

To examine the output characteristics of fabricated transistor, I_{DS}-V_{DS} variation (drain characteristics) was measured at different gate to source voltages. The characteristic curves were displayed at figure 3(a~c). From the figure, it was found that two different regions such as linear and saturation were observed.

At low drain voltage, between 0V to 4V, the drain current increased linearly with increase in drain voltages. In this region, the FET exhibited a resistive characteristics with the resistance as a function of the gate voltage. The drain current I_D increased with increase in drain voltage V_D and become saturated at the pinch-off point. After that, the I_D did not increase whereas increased in drain voltage V_D, which showed saturated or constant region.

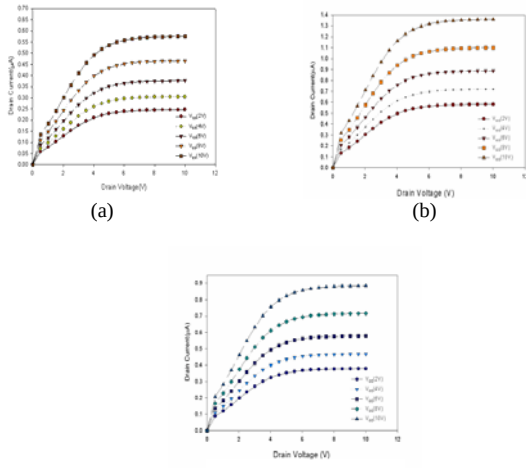
Moreover, the drain current was also enhanced with increasing gate voltages. So fabricated transistor was only operated in E-mode (enhancement-mode).

From drain characteristic curve, the drain current did not allowed to flow when the drain voltage approached zero. On the other hand, the drain current was zero if zero-bias gate voltage was applied. These facts showed the fabricated FeFET had normally- off nature.

To examine the device quality, (I_{DS}-V_{GS} variation), transfer characteristics were essentially observed at saturation-mode. These graphs were shown in Fig 4 (a~c). From the figure, it was seen that the I_{DS} was exponentially increased with gate voltage.

All transfer curves were varied gate potential with threshold voltage. All threshold voltages were found to be temperature influence and these were listed in Table 3.

To identify the transconductance value, $I_D^{1/m}$ was characterized with V_{GS} and shown in Fig.5 (a~c). From the characteristic



(a) (b)

(c)

Fig. 3 Drain characteristic of PTA-gated FET (a) at 500°C (b) at 600°C and (c) at 700°C

The largest maximum drain current was caused by the cell at 700˚C. To check the parabolic nature of transfer curve (or) the I_{DS} and (V_{GS} -V_{TH}) variation, m^{th} power of (V_{GS} -V_{TH}) was essentially studied by two unknown equations

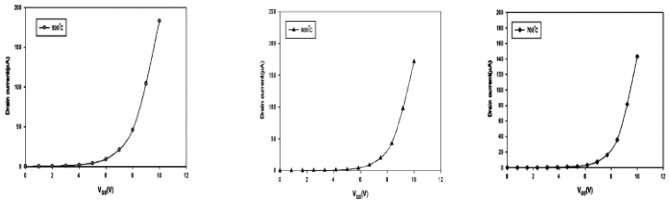
$$I_{DS} = K (V_{GS}-V_{TH})^m$$

Where I_{DS}= drain current
K= constant
V_{GS}= gate to source voltage
V_{TH}= threshold voltage

At V_{GS} = 6V, V_{TH} = 3.44 V, I_{DS} = 5.6 μA
V_{GS} = 7V, V_{TH} = 3.44 V, I_{DS} = 11 μA

$$5.6 = K (6 - 3.44)^m \quad (1)$$
$$11 = K (7 - 3.44)^m \quad (2)$$

Eqn (2) / (1), m =2.04 for the cell at 500ºC. The m^{th} power values were collected in Table 3.



(a) (b) (c)

Fig. 4 Transfer characteristics of PTA-gated FET (a) at 500°C (b) at 600°C and (c) at 700°C

curve, $I_D^{1/m}$ was linearly enhanced when the gate to source voltage was increased. The slope gave its transconductance value. The g_m value was measured by equation g_m=ΔI_D / ΔV_{GS}.A large transconductance was desirable to minimize the gate drive and provided high power gain. These values were organized and quoted in Table 3.

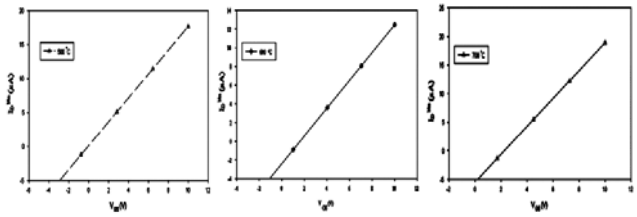


Fig. 5 Transconductance characteristics of PTA gated FET (a) at 500°C (b) at 600°C and (c) at 700°C in saturation mode.

Table 3 V_{TH}, $I_{D,max}$, m^{th} power and g_m at different process temperatures

Process Temperature	500°C	600°C	700°C
V_{TH}(V)	**3.44**	**3.33**	**4.33**
I_{Dmax}(μA)	**0.57**	**0.88**	**1.37**
m^{th} power	**2.04**	**1.95**	**2.11**
g_m(μS)	**1.7561**	**1.4853**	**2.4405**

4. CONCLUSION

Al (6mol%) doped $PbTiO_3$ powder (PTA6) was successfully formed by high temperature solid state reaction route. The great deal of information was obtained from the C^{-2} vs V characteristics. All straight line graphs were clearly found and indicated the film homogeneity of MFIS cells. From hysteresis loop characteristics, it was found that the polarization significantly depended on the electric field. So the capacitance and charge were also influenced by electric field. Thus all PTA 6 films exhibited the ferroelectricity at given process temperatures. From the output characteristics curve, the fabricated cells were only operated in E mode. The normally- off nature was found on drain characteristics curve too. From the transfer characteristics, I_{DS} and V_{GS} graph was found to be parabolic nature. $I_D^{1/m}$ and V_{GS} graph was examined to be linear relationship. The measurement m^{th} power values were range from 1.95 to 2.11. This fact gave the parabolic nature of transfer curve for fabricated cell. The slope of $I_D^{1/m}$ and V_{GS} graph gave the transconductance value of fabricated cell. Thus, the present research allowed more economical coating, techanical simplicity and easy adaptability. Moreover, the films fabricated with sol-based method were quite promising candidate for memory device applications.

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